

CLAIMS

What is claimed is:

- 1 1. A system comprising:
 - 2 a radio frequency integrated circuit including
 - 3 a single bit modulator to convert an analog
 - 4 signal into a serial digital bit stream, and
 - 5 an output driver coupled to the single bit
 - 6 sigma delta modulator, the output driver to drive
 - 7 the serial digital bit stream out from the radio
 - 8 frequency integrated circuit;
 - 9 and
 - 10 a digital signal processing integrated circuit
 - 11 including
 - 12 an input receiver coupled to the output
 - 13 driver of the radio frequency integrated circuit,
 - 14 the input receiver to receive the serial digital
 - 15 bit stream, and
 - 16 a decimator coupled to the input receiver,
 - 17 the decimator to receive the serial digital bit
 - 18 stream, lower a sampling rate of the serial
 - 19 digital bit stream and convert the serial digital
 - 20 bit stream into parallel digital data samples.
- 1 2. The system of claim 1, wherein
 - 2 the digital signal processing integrated circuit
 - 3 further includes
 - 4 a demodulator to digitally demodulate the
 - 5 parallel digital data samples into data words for

6 further signal processing by the digital signal
7 processing integrated circuit.

1 3. The system of claim 1, wherein
2 the single bit modulator is a single bit sigma
3 delta modulator.

1 4. The system of claim 1, wherein
2 the single bit modulator is a single bit delta
3 modulator.

1 5. The system of claim 1, wherein
2 the single bit modulator is a single bit analog to
3 digital converter and a modulator coupled together.

1 6. The system of claim 1, wherein
2 the output driver has a low voltage output swing,
3 the output driver to drive the serial digital bit
4 stream out of the radio frequency integrated circuit
5 with the low voltage output swing.

1 7. The system of claim 6, wherein
2 the input receiver to receive the serial digital
3 bit stream with the low voltage output swing.

1 8. The system of claim 7, wherein
2 the input receiver further to increase the low
3 voltage output swing of the serial digital bit stream
4 within the digital signal processing integrated
5 circuit.

1 9. The system of claim 6, wherein

2 the low voltage output swing between a high logic
3 level and a low logic level is less than an output
4 swing between a high logic level and a low logic level
5 of a three volt complementary metal oxide semiconductor
6 (CMOS) process technology.

1 10. The system of claim 6, wherein

2 the low voltage output swing between a high logic
3 level and a low logic level is less than an output
4 swing between a high logic level of 1.8 volts and a low
5 logic level of 0.2 volts.

1 11. The system of claim 8, wherein

2 the output driver translates first voltage levels
3 of a first output voltage swing of the serial digital
4 bit stream into second voltage levels with a second
5 output voltage swing less than the first output voltage
6 swing, and

7 the input receiver translates the second voltage
8 levels of the second output voltage swing into third
9 voltage levels with a third output voltage swing
10 greater than the second output voltage swing.

1 12. The system of claim 11, wherein

2 the third voltage levels are substantially the
3 same as the first voltage levels.

1 13. The system of claim 1, wherein

2 the output driver is double ended and generates a
3 differential signal to represent the serial digital bit
4 stream, and

5 the input receiver has a differential input to
6 receive the differential signal to represent the serial
7 digital bit stream.

1 14. The system of claim 13, wherein
2 the output driver is a low voltage differential
3 signaling transmitter to generate a low voltage
4 differential output signal with a low voltage
5 differential swing, and
6 the input receiver is a low voltage differential
7 signaling receiver to receive the low voltage
8 differential output signal with the low voltage
9 differential swing.

1 15. The system of claim 14, wherein
2 the low voltage differential swing is at least 100
3 milli-volts.

1 16. The system of claim 1, wherein
2 the serial digital bit stream is a rectangular
3 waveform.

1 17. The system of claim 1, wherein
2 the radio frequency integrated circuit is a
3 receiver.

1 18. The system of claim 1, wherein
2 the radio frequency integrated circuit is a
3 transceiver.

1 19. The system of claim 1, wherein

2 a delta sigma clock is coupled to the single bit
3 sigma delta modulator, a frequency of the delta sigma
4 clock to provide a data rate in the serial digital bit
5 stream.

1 20. The system of claim 19, wherein

2 the frequency of the delta sigma clock is
3 programmable to provide various data rates in the
4 serial digital bit stream for various wireless
5 communication systems.

1 21. The system of claim 1, wherein

2 a low frequency reference clock couples between
3 the radio frequency integrated circuit and the digital
4 signal processing integrated circuit to synchronize
5 clock signals of each.

1 22. The system of claim 21, wherein

2 the low frequency reference clock synchronizes a
3 sigma delta clock of the radio frequency integrated
4 circuit with a local clock of the digital signal
5 processing integrated circuit.

1 23. A radio frequency integrated circuit comprising:

2 at least one gain amplifier to couple to an
3 antenna to receive a first wireless radio frequency
4 signal of a first selectable carrier frequency;

5 at least one down converter coupled to the at
6 least one gain amplifier, the at least one down
7 converter to extract a first analog signal from the
8 first wireless radio frequency signal;

9 at least one single bit sigma delta modulator
10 coupled to the at least one down converter, the at
11 least one single bit sigma delta modulator to convert
12 the first analog signal into a first serial digital bit
13 stream; and

14 at least one output driver coupled to the at least
15 one single bit sigma delta modulator, the at least one
16 output driver to provide a low voltage output swing of
17 the first serial digital bit stream to reduce noise
18 generation as the first serial digital bit stream is
19 coupled to another integrated circuit.

1 24. The radio frequency integrated circuit of claim 23,
2 further comprising

3 a second gain amplifier to couple to the antenna
4 to simultaneously receive a third wireless radio
5 frequency signal of a third selectable carrier
6 frequency;

7 a second down converter coupled to the second gain
8 amplifier, the second down converter to extract a third
9 analog signal from the third wireless radio frequency
10 signal;

11 a second single bit sigma delta modulator coupled
12 to the second down converter, the second single bit
13 sigma delta modulator to convert the third analog
14 signal into a third serial digital bit stream; and

15 a second output driver coupled to the second
16 single bit sigma delta modulator, the second output
17 driver to provide a low voltage output swing of the
18 third serial digital bit stream to reduce noise

19 generation as the third serial digital bit stream is
20 coupled to another integrated circuit.

1 25. The radio frequency integrated circuit of claim 23,
2 wherein
3 the at least one gain amplifier is a variable gain
4 amplifier or a switched gain amplifier.

1 26. The radio frequency integrated circuit of claim 24,
2 wherein
3 the at least one gain amplifier and the second
4 gain amplifier are variable gain amplifiers or switched
5 gain amplifiers.

1 27. The radio frequency integrated circuit of claim 23,
2 wherein
3 the radio frequency integrated circuit is a radio
4 frequency receiver integrated circuit.

1 28. The radio frequency integrated circuit of claim 23,
2 wherein
3 the radio frequency integrated circuit is a
4 transceiver and further includes,
5 an input receiver to receive a second serial
6 digital bit stream to be transmitted;
7 a data recoverer coupled to the input
8 receiver, the data recoverer to recover digital
9 data bits from the second serial digital bit
10 stream;

11 a low pass filter coupled to the data
12 recoverer, the low pass filter to convert the
13 digital data bits into a second analog signal;
14 a mixer coupled to the low pass filter, the
15 mixer to up-convert the second analog signal from
16 a baseband frequency to a second selectable
17 carrier frequency as a second wireless radio
18 frequency signal; and
19 an amplifier coupled to the mixer, the
20 amplifier to amplify the second wireless radio
21 frequency signal for broadcast over the antenna.

1 29. The radio frequency integrated circuit of claim 28,
2 wherein

3 the first selected carrier frequency and the
4 second selected carrier frequency are selected from a
5 set of carrier frequencies of a first selected wireless
6 communication system.

1 30. The radio frequency integrated circuit of claim 29,
2 wherein

3 the selected wireless communication system is
4 selected from the set of Universal Mobile
5 Telecommunication System (UMTS), Global System for
6 Multiple Communication (GSM), GSM Mobile Application
7 Part (GSM-MAP), General Packet Radio Protocol System or
8 General Packet Radio Service (GPRS), Enhanced Data GSM
9 Environment (EDGE), (GAIT), Orthogonal Frequency-
10 Division Multiplexing (OFDM), Code Orthogonal Frequency
11 Division Multiplexing (COFDM), Block Coding,
12 Convolutional Coding, Turbo Coding, Trellis Coding,

13 Gaussian Minimum Shift Keying (GMSK), Quadrature Phase
14 Shift Keying (QPSK), Quadrature Amplitude Modulation
15 (QAM), Frequency Modulation (FM), Frequency Division
16 Multiple Access (FDMA), Time Division Multiple Access
17 (TDMA), Code Division Multiple Access (CDMA),
18 Narrowband CDMA (N-CDMA), Wideband CDMA (W-CDMA),
19 CDMA2000, CDMA2000-1XEV, CDMA2000-EVDO, CDMA2000-EDV,
20 Time Division-Synchronized Code Division Multiple
21 Access (TD-SCDMA), Third-Generation Partnership Project
22 (3GPP TDD), International Mobile Telecommunication
23 (IMT), IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC,
24 Personal Communication System (PCS), Digital
25 Communication System (DCS), Personal Digital Cellular
26 (PDC), Digital Enhanced Cordless Telecommunications
27 (DECT), Advanced Mobile Phone System (AMPS), Wireless
28 Local Area Network (LAN) (IEEE 802.11a, IEEE 802.11b,
29 IEEE 802.11g), and Global Positioning System (GPS).

1 31. The radio frequency integrated circuit of claim 29,
2 wherein
3 the first selected carrier frequency is selected
4 from a set of carrier frequencies of a Universal Mobile
5 Telecommunication System (UMTS), Global System for
6 Multiple Communication (GSM), GSM Mobile Application
7 Part (GSM-MAP), General Packet Radio Protocol System or
8 General Packet Radio Service (GPRS), Enhanced Data GSM
9 Environment (EDGE), (GAT), Orthogonal Frequency-
10 Division Multiplexing (OFDM), Code Orthogonal Frequency
11 Division Multiplexing (COFDM), Gaussian Minimum Shift
12 Keying (GMSK), Quadrature Phase Shift Keying (QPSK),
13 Quadrature Amplitude Modulation (QAM), Frequency

14 Modulation (FM), Frequency Division Multiple Access
15 (FDMA), Time Division Multiple Access (TDMA), Code
16 Division Multiple Access (CDMA), Narrowband CDMA (N-
17 CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV,
18 CDMA2000-EVDO, CDMA2000-EDV, Time Division-Synchronized
19 Code Division Multiple Access (TD-SCDMA), Third-
20 Generation Partnership Project (3GPP TDD),
21 International Mobile Telecommunication (IMT),
22 IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC, Personal
23 Communication System (PCS), Digital Communication
24 System (DCS), Personal Digital Cellular (PDC), Digital
25 Enhanced Cordless Telecommunications (DECT), Advanced
26 Mobile Phone System (AMPS), Wireless Local Area Network
27 (LAN) (IEEE 802.11a, IEEE 802.11b, IEEE 802.11g), and
28 Global Positioning System (GPS), and

29 the second selected carrier frequency is selected
30 from a set of carrier frequencies of Universal Mobile
31 Telecommunication System (UMTS), Global System for
32 Multiple Communication (GSM), GSM Mobile Application
33 Part (GSM-MAP), General Packet Radio Protocol System or
34 General Packet Radio Service (GPRS), Enhanced Data GSM
35 Environment (EDGE), (GAT), Orthogonal Frequency-
36 Division Multiplexing (OFDM), Code Orthogonal Frequency
37 Division Multiplexing (COFDM), Gaussian Minimum Shift
38 Keying (GMSK), Quadrature Phase Shift Keying (QPSK),
39 Quadrature Amplitude Modulation (QAM), Frequency
40 Modulation (FM), Frequency Division Multiple Access
41 (FDMA), Time Division Multiple Access (TDMA), Code
42 Division Multiple Access (CDMA), Narrowband CDMA (N-
43 CDMA), Wideband CDMA (W-CDMA), CDMA2000, CDMA2000-1XEV,
44 CDMA2000-EVDO, CDMA2000-EDV, Time Division-Synchronized

45 Code Division Multiple Access (TD-SCDMA), Third-
46 Generation Partnership Project (3GPP TDD),
47 International Mobile Telecommunication (IMT),
48 IMT2000MC, IMT2000DS, IMT2000SC, IMT2000TC, Personal
49 Communication System (PCS), Digital Communication
50 System (DCS), Personal Digital Cellular (PDC), Digital
51 Enhanced Cordless Telecommunications (DECT), Advanced
52 Mobile Phone System (AMPS), and Wireless Local Area
53 Network (LAN) (IEEE 802.11a, IEEE 802.11b, IEEE
54 802.11g).

1 32. A radio frequency integrated circuit comprising:
2 an input receiver to receive a serial digital
3 transmission bit stream with a reduced output voltage
4 swing, the input receiver to increase the output
5 voltage swing of the serial digital transmission bit
6 stream in the radio frequency integrated circuit;
7 a data recoverer coupled to the input receiver,
8 the data recoverer to recover digital data bits from
9 the serial digital transmission bit stream;
10 a low pass filter coupled to the data recoverer,
11 the low pass filter to convert the digital data bits
12 into an analog transmission signal;
13 a mixer coupled to the low pass filter, the mixer
14 to up-convert the analog transmission signal from a
15 baseband frequency to a selectable carrier frequency as
16 a transmit radio frequency signal; and
17 an amplifier coupled to the mixer, the amplifier
18 to amplify the transmit radio frequency signal for
19 broadcast over an antenna.

1 33. The radio frequency integrated circuit of claim 32,
2 wherein
3 the radio frequency integrated circuit is a
4 transmitter.

1 34. A method for a wireless radio, the method comprising:
2 receiving a first wireless radio signal;
3 extracting a first analog signal from the first
4 wireless radio signal;
5 converting the first analog signal into a first
6 serial digital data signal;
7 providing a low voltage output swing in the first
8 serial digital data signal; and
9 transmitting the first serial digital data signal
10 with the low voltage output swing from a radio
11 frequency (RF) integrated circuit to a digital signal
12 processing (DSP) integrated circuit.

1 35. The method of claim 34, further comprising:
2 receiving a second wireless radio signal;
3 extracting a second analog signal from the second
4 wireless radio signal;
5 converting the second analog signal into a second
6 serial digital data signal;
7 providing a low voltage output swing in the second
8 serial digital data signal; and
9 transmitting the second serial digital data signal
10 with the reduced output voltage swing from the radio
11 frequency integrated circuit to the digital signal
12 processing (DSP) integrated circuit.

1 36. The method of claim 35, wherein
 2 the first wireless radio signal and the second
 3 wireless radio signal are simultaneously received.

1 37. The method of claim 35, wherein
 2 the first analog signal and the second analog
 3 signal are simultaneously extracted.

1 38. The method of claim 35, wherein
 2 the first wireless radio signal is received during
 3 the time period that the second wireless radio signal
 4 is received.

1 39. The method of claim 35, wherein
 2 the first analog signal is extracted during the
 3 time period that the second analog signal is extracted.

1 40. The method of claim 35, further comprising:
 2 receiving a third wireless radio signal;
 3 extracting a third analog signal from the third
 4 wireless radio signal;
 5 converting the third analog signal into a third
 6 serial digital data signal;
 7 providing a low voltage output swing in the third
 8 serial digital data signal; and
 9 transmitting the third serial digital data signal
 10 with the low output voltage swing from a radio
 11 integrated circuit to a digital signal processing (DSP)
 12 integrated circuit.

1 41. The method of claim 40, wherein
2 the first wireless radio signal, the second
3 wireless radio signal, and the third wireless radio
4 signal are simultaneously received.

1 42. The method of claim 41, wherein
2 the first analog signal, the second analog signal,
3 and the third analog signal are simultaneously
4 extracted.

1 43. The method of claim 34, further comprising:
2 receiving the first serial digital data signal
3 with the reduced output voltage swing;
4 increasing the output voltage swing in the first
5 serial digital data signal;
6 reducing a sampling frequency of the first serial
7 digital data signal; and
8 converting the first serial digital data signal
9 into a parallel digital data signal for processing by
10 the DSP integrated circuit.

1 44. The method of claim 34, wherein
2 the converting of the first analog signal into the
3 first serial digital data signal is a delta-sigma
4 modulation of the first analog signal into the first
5 serial digital data signal.

1 45. The method of claim 43, further comprising:

2 recovering data words from the parallel digital
3 data signal by digital demodulation for a predetermined
4 wireless communication system.

1 46. The method of claim 34, wherein
2 the transmitting of the first serial digital data
3 signal is over a single wire.

1 47. The method of claim 34, wherein
2 the first serial digital data signal is a
3 differential data signal, and
4 the transmitting of the first serial digital data
5 signal is over a pair of wires.

1 48. The method of claim 34, wherein
2 the first serial digital data signal is a complex
3 differential data signal and the transmitting of the
4 first serial digital data signal is over two pairs of
5 wires,
6 a first differential data signal of the first
7 serial digital data signal is transmitted over the
8 first pair of wires, and
9 a second differential data signal of the
10 first serial digital data signal is transmitted
11 over the second pair of wires.

1 49. The method of claim 48, wherein
2 the first differential data signal is a real
3 component of a complex data signal, and
4 the second differential data signal is an
5 imaginary component of the complex data signal.

1 50. The method of claim 48, wherein
2 the first differential data signal is an in-phase
3 signal, and
4 the second differential data signal is a
5 quadrature signal with respect to the in-phase signal.

1 51. The method of claim 34, wherein
2 the first serial digital data signal is a
3 multiphase differential data signal and the
4 transmitting of the first serial digital data signal is
5 over two pairs of wires,
6 a magnitude data signal of the first serial
7 digital data signal is transmitted over the first
8 pair of wires, and
9 a phase data signal of the first serial
10 digital data signal is transmitted over the second
11 pair of wires.

1 52. The method of claim 34, further comprising:
2 receiving a fourth serial digital data signal from
3 the DSP integrated circuit for transmission over a
4 wireless communication system;
5 converting the fourth serial digital data signal
6 from the DSP integrated circuit into a fourth analog
7 signal;
8 up-converting the fourth analog signal to a
9 selectable carrier frequency; and
10 transmitting the fourth analog signal through the
11 antenna as a fourth wireless radio frequency signal.

1 53. The method of claim 52, wherein
2 the fourth serial digital data signal from the DSP
3 integrated circuit is a low voltage output swing
4 signal, and the method further includes
5 increasing the low voltage output swing in the
6 fourth serial digital data signal from the DSP
7 integrated circuit.

1 54. A data signal flow between a radio frequency integrated
2 circuit and a digital signal processing (DSP) integrated
3 circuit, the data signal flow comprising:
4 a first serial digital data signal flowing from
5 the radio frequency integrated circuit to the DSP
6 integrated circuit, the first serial digital data
7 signal representing a first received data signal from a
8 first wireless communication system; and
9 a second serial digital data signal flowing from
10 the radio frequency integrated circuit to the DSP
11 integrated circuit, the second serial digital data
12 signal representing a second received data signal from
13 a second wireless communication system.

1 55. The data signal flow of claim 54, wherein
2 the first serial digital data signal is a complex
3 differential data signal flowing over two pairs of
4 wires,
5 an in-phase differential data signal of the
6 first serial digital data signal flows over a
7 first pair of wires, and

8 a quadrature differential data signal with
9 respect to the in-phase differential data signal
10 of the first serial digital data signal flows over
11 a second pair of wires.

1 56. The data signal flow of claim 54, wherein
2 the first serial digital data signal is a
3 multiphase differential data signal flowing over two
4 pairs of wires,
5 a magnitude data signal of the first serial
6 digital data signal flows over a first pair of
7 wires, and
8 a phase data signal of the first serial
9 digital data signal flows over a second pair of
10 wires.

1 57. The data signal flow of claim 54, further comprising:
2 a third serial digital data signal flowing from
3 the DSP integrated circuit to the radio frequency
4 integrated circuit, the third serial digital data
5 signal representing a first transmit data signal for
6 communication over the first wireless communication
7 system.

1 58. The data signal flow of claim 57, wherein
2 the third serial digital data signal is a complex
3 differential data signal flowing over two pairs of
4 wires,
5 an in-phase differential data signal of the
6 third serial digital data signal flows over a
7 first pair of wires, and

8 a quadrature differential data signal with
9 respect to the in-phase differential data signal
10 of the third serial digital data signal flows over
11 a second pair of wires.

1 59. The data signal flow of claim 57, wherein
2 the third serial digital data signal is a
3 multiphase differential data signal flowing over two
4 pairs of wires,
5 a magnitude data signal of the third serial
6 digital data signal flows over a first pair of
7 wires, and
8 a phase data signal of the third serial
9 digital data signal flows over a second pair of
10 wires.

1 60. The data signal flow of claim 54, wherein
2 the first serial digital data signal is a low
3 voltage differential data signal flowing over at least
4 one pair of wires.

1 61. The data signal flow of claim 57, wherein
2 the third serial digital data signal is a low
3 voltage differential data signal flowing over at least
4 one pair of wires.

1 62. The data signal flow of claim 54, wherein
2 a data rate of the first serial digital data
3 signal is variable to adapt to a selected wireless
4 communication system.

1 63. The data signal flow of claim 57, wherein

2 a data rate of the first serial digital data
3 signal, a data rate of the second serial digital data
4 signal, and a data rate of the third serial digital
5 data signal are variable to adapt to selected wireless
6 communication systems.

1 64. The data signal flow of claim 54, wherein
2 the first serial digital data signal and the
3 second serial digital data signal simultaneously flow
4 from the radio frequency integrated circuit to the DSP
5 integrated circuit to simultaneously receive data over
6 two wireless channels of communication.

1 65. The data signal flow of claim 57, wherein
2 the first serial digital data signal, the second
3 serial digital data signal, and the third serial
4 digital data signal simultaneously flow between the
5 radio frequency integrated circuit and the DSP
6 integrated circuit to
7 simultaneously receive data over two wireless
8 channels of communication and
9 simultaneously transmit data over one
10 wireless channel of communication.

1 66. A radio frequency integrated circuit comprising:
2 a plurality of gain amplifiers to couple to an
3 antenna to simultaneously receive wireless radio
4 frequency signals of selectable carrier frequencies;
5 a plurality of down converters coupled to the
6 plurality of gain amplifiers, the plurality of down
7 converters to simultaneously extract analog signals
8 from the wireless radio frequency signals; and

9 a plurality of sigma delta modulators coupled to
10 the plurality of down converters, the plurality of
11 single bit sigma delta modulators to simultaneously
12 convert the analog signals into serial digital bit
13 streams; and

14 a plurality of output drivers coupled to the
15 plurality of single bit sigma delta modulators, the
16 plurality of output drivers to couple the serial
17 digital bit streams to another integrated circuit.

1 67. The radio frequency integrated circuit of claim 66,
2 wherein,

3 the plurality of output drivers further to reduce
4 an output voltage swing of the serial digital bit
5 streams to further reduce noise generation as the
6 serial digital bit streams are coupled to the another
7 integrated circuit.

1 68. The radio frequency integrated circuit of claim 66,
2 wherein

3 the plurality of gain amplifiers are a variable
4 gain amplifier or a switched gain amplifier.

1 69. The radio frequency integrated circuit of claim 66,
2 wherein

3 the radio frequency integrated circuit is a
4 transceiver and further includes,
5 an input receiver to receive a serial digital
6 transmission bit stream from the another
7 integrated circuit;

8 a data recoverer coupled to the input
9 receiver, the data recoverer to recover digital
10 data bits from the serial digital transmission bit
11 stream;
12 a low pass filter coupled to the data
13 recoverer, the low pass filter to convert the
14 digital data bits into an analog transmission
15 signal;
16 a mixer coupled to the low pass filter, the
17 mixer to up-convert the analog transmission signal
18 from a baseband frequency to a second selectable
19 carrier frequency as a transmit radio frequency
20 signal; and
21 an amplifier coupled to the mixer, the
22 amplifier to amplify the transmit radio frequency
23 signal for broadcast over the antenna.

1 70. The radio frequency integrated circuit of claim 69,
2 wherein,
3 the serial digital transmission bit stream has a
4 reduced output voltage swing to further reduce noise,
5 and
6 the input receiver to increase the output voltage
7 swing of the serial digital transmission bit stream in
8 the radio frequency integrated circuit.

1 71. A system comprising:
2 a radio frequency integrated circuit including
3 a single bit sigma delta modulator with an
4 analog input and a serial digital output, and

5 an output driver having an input coupled to
6 the serial digital output of the single bit sigma
7 delta modulator, the output driver having a
8 differential output;
9 and
10 a digital signal processing integrated circuit
11 including
12 an input receiver coupled to the output
13 driver of the radio frequency integrated circuit,
14 the input receiver having a differential input to
15 couple to the differential output of the output
16 driver, the input receiver having a serial digital
17 output.

1 72. The system of claim 71, wherein
2 the output driver to drive a serial digital bit
3 stream out from the radio frequency integrated circuit
4 with a low voltage differential output swing to lower
5 noise.

1 73. The system of claim 72, wherein
2 the input receiver to receive the serial digital
3 bit stream with the low voltage differential output
4 swing.

1 74. The system of claim 71, wherein
2 the digital signal processing integrated circuit
3 further includes
4 a decimator coupled to the serial digital
5 output of the input receiver, the decimator having
6 a parallel digital output, and

7 a demodulator coupled to the parallel digital
8 output of the decimator.

1 75. A radio frequency integrated circuit comprising:
2 a gain amplifier having an input to couple to an
3 antenna, the gain amplifier having an analog output;
4 a down converter having an analog input coupled to
5 the analog output of the gain amplifier, the down
6 converter having an analog output;
7 a single bit sigma delta modulator having an
8 analog input coupled to the analog output of the down
9 converter, the single bit sigma delta modulator having
10 a serial digital output; and
11 an output driver having an input coupled to the
12 serial digital output of the single bit sigma delta
13 modulator, the output driver having a differential
14 output.

1 76. The radio frequency integrated circuit of claim 75,
2 wherein
3 the radio frequency integrated circuit is a radio
4 frequency receiver integrated circuit.

1 77. The radio frequency integrated circuit of claim 75,
2 wherein
3 the radio frequency integrated circuit is a
4 transceiver and further includes,
5 an input receiver having a differential
6 input, the input receiver having a serial digital
7 output;

8 a data recoverer having an input coupled to
9 the serial digital output of the input receiver,
10 the data recoverer having a serial digital output;
11 a low pass filter having an input coupled to
12 the serial digital output of the data recoverer,
13 the low pass filter having an analog output;
14 a mixer having an input coupled to the analog
15 output of the low pass filter, the mixer having an
16 analog output; and
17 an amplifier having an input coupled to
18 analog output of the mixer, the amplifier having
19 an output to couple to the antenna.

1 78. A system comprising:
2 a radio frequency integrated circuit including
3 a modulating analog to digital converter with
4 a single bit output, the modulating analog to
5 digital converter to convert an analog input
6 signal into a serial digital bit output stream,
7 and
8 an output driver coupled to the single bit
9 analog to digital converter, the output driver to
10 drive the serial digital bit stream out from the
11 radio frequency integrated circuit;
12 and
13 a processor coupled to the radio frequency
14 integrated circuit.

1 79. The system of claim 78, wherein
2 the processor includes

3 an input receiver coupled to the output
4 driver of the radio frequency integrated circuit,
5 the input receiver to receive the serial digital
6 bit stream.

1 80. The system of claim 79, wherein
2 the processor is a digital signal processor and
3 further includes
4 a decimator coupled to the input receiver,
5 the decimator to receive the serial digital bit
6 stream, lower a sampling rate of the serial
7 digital bit stream, and convert the serial digital
8 bit stream into parallel digital data samples, and
9 a demodulator to digitally demodulate the
10 parallel digital data samples into data words for
11 further signal processing by the digital signal
12 processing integrated circuit.

1 81. The system of claim 79, wherein
2 the processor includes programmable instructions
3 to provide
4 a decimator coupled to the input receiver,
5 the decimator to receive the serial digital bit
6 stream, lower a sampling rate of the serial
7 digital bit stream, and convert the serial digital
8 bit stream into parallel digital data samples; and
9 a demodulator coupled to the decimator, the
10 demodulator to digitally demodulate the parallel
11 digital data samples into data words for further
12 signal processing by the digital signal processing
13 integrated circuit.

1 82. A system comprising:
2 a radio frequency integrated circuit including
3 a modulating analog to digital converter with
4 an analog input and a serial digital output, and
5 an output driver having an input coupled to
6 the serial digital output of the modulating analog
7 to digital converter, the output driver having a
8 digital output;
9 and
10 a processor coupled to the radio frequency
11 integrated circuit.

1 83. The system of claim 82, wherein
2 the processor includes
3 an input receiver coupled to the digital
4 output of the output driver of the radio frequency
5 integrated circuit, the input receiver having a
6 digital input to couple to the digital output of
7 the output driver, the input receiver having a
8 serial digital output.

1 84. The system of claim 83, wherein
2 the processor is a digital signal processor and
3 further includes
4 a decimator coupled to the serial digital
5 output of the input receiver, the decimator having
6 a digital output, and
7 a demodulator coupled to the digital output
8 of the decimator.

1 85. The system of claim 83, wherein
2 the processor includes programmable instructions
3 to provide
4 a decimator coupled to the serial digital
5 output of the input receiver, the decimator having
6 a digital output, and
7 a demodulator coupled to the digital output
8 of the decimator.